

Semiconductor Memory with Wordline Timing

Abstract of the Disclosure

5 A semiconductor memory with wordline timing, which links activating a wordline to an isolation signal. The isolation signal is applied to a memory section adjacent the memory section containing the wordline to be activated. Upon such an isolation signal shifting low and isolating the adjacent memory section, a timing circuit triggers a wordline decoder to activate a select wordline. The timing circuit prevents activation of the wordline decoder until the isolation signal is received.

"Express Mail" mailing label number: EL671641471US

Date of Deposit: June 14, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

09031472 061401
T04T90 24T880